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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,857	06/07/2005	Assaf Shappir	ELGP-6715-US	7211

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

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07/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/537,857	SHAPPIR ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to communication filed on 6/5/07. Claims 1 – 19 are pending on this application. Claims 1, 9 and 19 are independent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 - 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chindalore et al., U.s. patent No. 6,839,280 B1 – filed: Jun. 27, 2003.

Regarding independent claim 1, Fig. 2 of Chindalore et al. discloses a method of erasing (22) one or more non-volatile memory ("NVM") cells (Fig. 5) comprising: applying to the one or more NVM cells (Fig. 5) an erase pulse (22) having a substantially non-flat voltage profile (22, Fig. 2 disclosing erase voltage with non-flat, Col. 3 lines 19 – 23; See explained below, under Response to Argument).

Regarding dependent claim 2, Chindalore et al. disclose the method according to claim 1, wherein the voltage profile of the erase pulse (22) is predefined (inherent to circuit because in order to perform function of erasing, every erase voltage have to be defined).

Regarding to dependent claim 3, Chindalore et al. disclose the method according to claim 2, wherein the erase pulse (22) has a voltage profile selected from

the group consisting of ramp-like, trapezoida, exponential-growth –like, asymptote-like and stepped (22, Fig. 2 disclosing ramp-like, exponential-growth –like, asymptote-like).

Regarding dependent claim 4, Chindalore et al. disclose the method according to claim 3, wherein the erase pulse (22) is applied to each sub-set (50, 58; 56,60 of Fig. 5) of the set of NVM cells in a staggered sequence (50,58; 56,60 of Fig. 5).

Regarding dependent claim 5, Chindalore et al. disclose the method according to claim 1, wherein the voltage profile of the erase pulse is dynamically adjusted based on feedback (col. 5 lines 1 – 7).

Regarding dependent claim 6, Chindalore et al. disclose the method according to claim 5, wherein the feedback comes from a sensor from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor (48, fig. 4 discloses a voltage derive sensor for IREF feedback to adjust the voltage programmed and erased voltage of Vcell; Col. 5 lines 1 – 7).

Regarding depending claim 7, Chindalore et al. disclose wherein the voltage of the erase pulse is adjusted in an inversion relation to the current measure by the current sensor (Col. 5 lines 1 – 7 of Chindalore et al. disclose current feedback sensor device 48 having voltage adjustment, which inversed relation with feedback current [decreasing reference current, resulting cell voltage increases over time as the memory is erased).

Regarding dependent claim 8, Chindalore et al. disclose wherein the voltage of the erase pulse is adjusted at a rate correlated to a signal produced by the current derivative sensor (Col. 5 lines 1 – 7 of Chindalore et al. disclose current feedback

sensor device 48 having voltage adjustment correlated to increase or decrease rate of current feedback I REF.

Regarding independent claim 9, Fig. 3 of Chindalore et al. discloses a circuit for erasing (Col. 3 lines 36 – 40) one or non-volatile memory cells (32) comprising, an erase pulse source (38) to produce an erase pulse (22, Fig. 2) having a substantially non-flat voltage profile (Col. 2 lines 20 – 24; See explained below, under Response to Argument)

Regarding dependent claim 10, Chindalore et al. disclose the circuit according to claim 9, wherein said erase pulse source comprises a charge-pump (Col. 3 line 10).

Regarding dependent claim 11, Chindalore et al. disclose the method according to claim 10, wherein the erase pulse (22) has a voltage profile selected from the group consisting of ramp-like, trapezoida, exponential-growth –like, asymptote-like and stepped (22, Fig. 2 disclosing ramp-like, exponential-growth –like, asymptote-like)

Regarding dependent claim 12, Chindalore et al. disclose the circuit according to claim 9, further comprising a cell select circuit (38) adapted to select to which cells of a set of NVM cells (32) the erase pulse is applied (22, Fig. 2).

Regarding dependent claim 13, Chindalore et al. disclose the circuit according to claim 12, wherein said cell select circuit (38) is adapted to apply the erase pulse to each sub-set (22, Fig. 2) of the set of NVM cells (32) in a staggered sequence (Fig. 5 50,58; 56,60).

Regarding dependent claim 14, Fig. 3 of Chindalore et al. discloses a circuit according to claim 9, further discloses comprising a sensor (this is a inherent device to

22, Fig. 2 of Chindalore et al. because a sensor device must be provided in order to discloses the erase voltage characteristic of 22, Fig. 2) to sense a characteristic of the erase pulse (22, Fig. 2) as it is being applied to the one or more NVM cells (32).

Regarding dependent claims 15 – 18, the claims incorporated the same subject matter as of claims 5 – 8, and rejected along the same rationale.

Regarding independent claim 19, Fig. 3 of Chindalore et al. discloses a system for erasing (col. 3 lines 36 – 40) one or non-volatile memory ("32") cells comprising: A NVM array (32), and an erase pulse source (38) to produce an erase pulse (Col. 3 lines 36 – 40) having a substantially non-flat voltage profile (22, Fig. 2; See explained below, under Response to Argument).).

Response to Arguments

3. Applicant's arguments filed 6/5/07 with respect to claims 1, 9 and 19 have been fully considered but they are not persuasive from the following:

Under remarks, applicant pointed to abstract of Chindalore et al. and argued "Chindalore does not teach an erase pulse having a substantial non-flat voltage profiled". Examiner respectful traverse because Fig. 4 of Chindalore teaches a memory cell (50, Col. 5 line 16) having a bias voltage Vcell, which is increased over time as the memory is erased as showed in Fig. 2 (Col. 5 lines 5 – 7). Therefore the bias Vcell is a non-constant or non–flat voltage (Fig. 2) for erasing the memory. Further more, "a non-flat voltage" as claimed is draw to a non-constant voltage, which means the voltage is change with respect to time, while Col. 5 lines 5 – 7 of Chindalore disclose the voltage

Vcell for erased the memory 50 is increased over time; therefore increase voltage of Vcell for erasing memory cell (Col. 5 lines 5 – 7) of Chindalore clearly teaches a "non-flat" voltage of claimed invention.

Per explained above, prior office action is applying to this office action.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

5. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's

supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 7/9/07

SON DINH
PRIMARY PATENT EXAMINER